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| **Digital Logic Design**  **(EL-227)** |
| **Spring-2020** |

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| **LAB 03**  **Universal Logic Gates** | | | | |
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| **NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), KARACHI** | | | | |
| Date: 22 Feb 2020 | | | | |
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**Lab Session 03: Universal Logic Gates**

**OBJECTIVES:**

The objectives of this lab is:

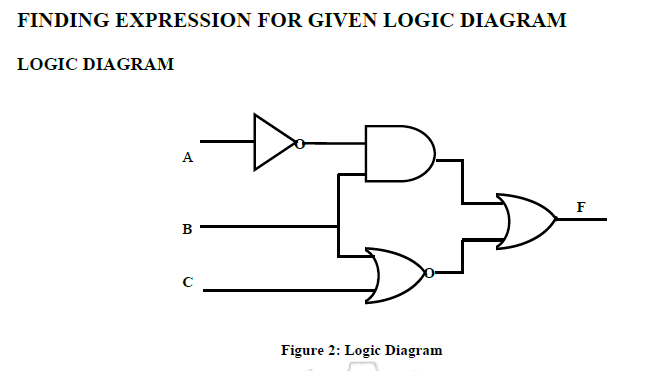
* To study the realization of basic gates using universal gates (NAND gate & NOR gate)
* To learn technology mapping (NAND-NAND & NOR-NOR implementation) and its significance in order to obtain cost effective circuit for implementation

**APPARATUS:**

* Logic trainer
* Logic probe

**COMPONENTS:**

ICs 74LS02, 74LS00 , Jumper Wire



**PROCEDURE**

1. Set the power supply to 5V. With the help of a multimeter check the voltage at the output knobs of the power supply.

2. Connect wires, long enough to reach the bread board, with the two knobs of the power supply. Again using millimeter, check the voltage at the non-connected end of the wires.

3. Insert ICs on the bread board and make their supply and ground connections.

4. As given in the logic diagram, make connections using wires and gates in the ICs.

5. Apply different combinations at the three inputs and observe the output

**OBSERVATION**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | EXPECTED OUTPUT | OBSERVED OUTPUT |
| 0 | 0 | 0 |  |  |
| 0 | 0 | 1 |  |  |
| 0 | 1 | 0 |  |  |
| 0 | 1 | 1 |  |  |
| 1 | 0 | 0 |  |  |
| 1 | 0 | 1 |  |  |
| 1 | 1 | 0 |  |  |
| 1 | 1 | 1 |  |  |

**Introduction:**

The design of a combinational circuit starts from the specification of the problem and culminates in a logic diagram or net-list that describes a logic diagram. The procedure involves the specification, formulation, optimization, & technology mapping.

Technology mapping is actually transformation of logic diagram or net-list to a new diagram using the available implementation technology. Typically NAND and NOR gates are more desirable to use in technology mapping due to the following reasons:

1. NAND and NOR gates are said to be universal gates where universal gate is a gate which can implement any Boolean function without needing any other type of gate.
2. Using universal gate in technology mapping may further reduce cost of optimized logic diagram.
3. Universal gates are easier to fabricate with electronic components.

A convenient way to implement a Boolean function with NAND gates only (NAND-NAND implementation) is to begin with the optimized logic diagram of the circuit consisting of AND, OR and NOT gates. The function is converted to pure NAND logic by replacing each gate in logic diagram with its representation using NAND gates only as shown in figure 5-1. After that, all inverter pairs are cancelled. The same conversion procedure is applied to implement a Boolean function with NOR gates only (NOR-NOR implementation).

**Universal Logic Gates:**

1. **NAND Gate:**

**“It is a device whose output is 1 if at least one or all of the inputs are low (0)”**

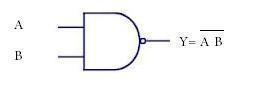
** Symbol:**

Figure 2 NAND Gate Symbol

**Function Table:**

|  |  |  |
| --- | --- | --- |
| **Inputs** | | **Output** |
| **A** | **B** | **Y** |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

Table: 1 NAND Gate Truth Table

H= Logic High, L= Logic Low

#### **Connection Diagram:**

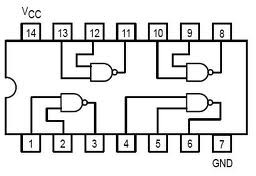
74LS00 IC contains four 2-input NAND gates. The connection diagram for this IC are shown below:

Figure 2 NAND Gate Connection diagram

1. **NOR Gate:**

***“It is a device whose output is 1 if all the given inputs are low (0)”.***

**Symbol:**

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Figure 3 NOR Gate Symbol

**Function Table:**

|  |  |  |
| --- | --- | --- |
| **Inputs** | | **Output** |
| **A** | **B** | **Y** |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

Table: 2 NOR Gate Truth Table

H= Logic High, L= Logic Low

#### **Connection Diagram:**

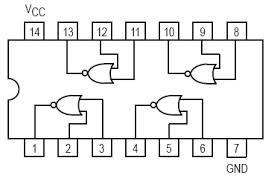
74LS02 IC contains four 2-input NOR gates. The function table and connection diagram for this IC are shown below:

Figure 4 NOR Gate Connection diagram

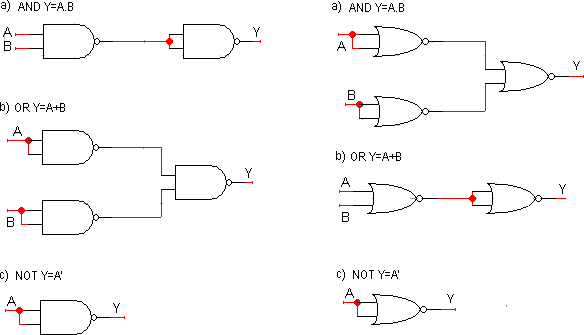
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Figure 5 NAND-NAND and NOR-NOR representation of basic logic gates

**Application of Universal Gates:**

### Burglar alarm

When the switch is closed one input of the NAND gate is LOW. When the LDR is in the light the other input is LOW. This means that if either of these things happen, i.e. the switch is closed or the light is on one of the inputs is LOW, the output is HIGH and the buzzer sounds.

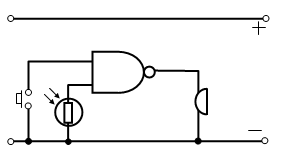
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Figure 6 NAND- Gate Based Burglar alarm

### Freezer warning buzzer

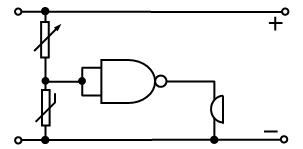
When the thermistor is COLD its resistance is LARGE and the input to the NAND gate is high.  
Since the NAND gate is connected as an INVERTER the output is LOW. As the thermostat warms up its resistance decreases, the voltage across it falls and the input to the NAND gate falls.

Figure 7 NAND- Gate Based Freezer warning buzzer

1. **Car Door Open System of an Automobile**

A car needs to be designed that the driver gets a visual indication if any of the doors of the car is open so that it helps to avoid accident and injury to the passengers. Assuming there are two doors (just for simplicity, it works for more doors as well) where this system is fitted, the circuit can be designed using a NAND gate as follows You can see from the figure that when any of the switches is open due to the door position, the NAND gate energies the lamp inside the car, hence warning the driver.

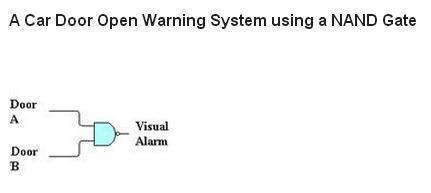
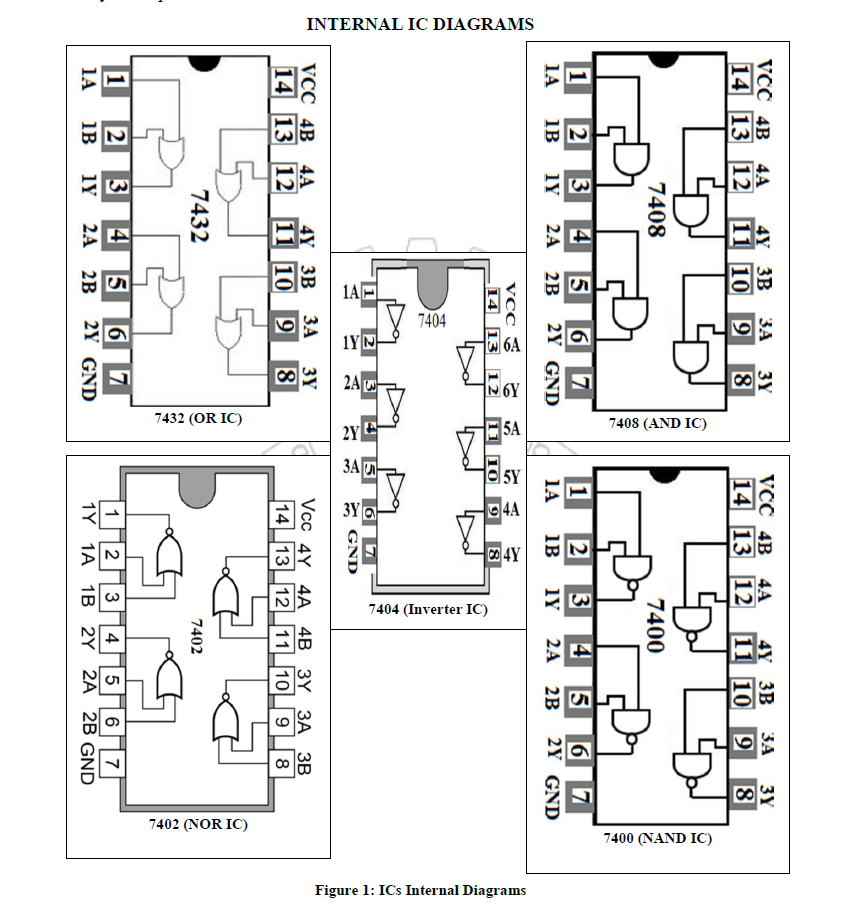
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Figure 8 NAND- Gate Based Car Open System of an Automobile

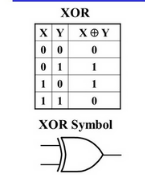
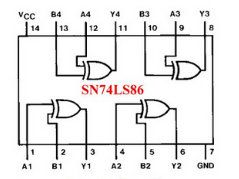


**Hardware connection**

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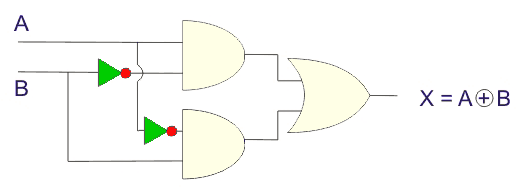
**XOR:**

An XOR gate (also known as an EOR, or EXOR gate) – pronounced as Exclusive OR gate – is a digital logic gate that gives a true (i.e. a HIGH or 1) output when the number of true inputs is odd. An XOR gate implements an exclusive OR, i.e., a true output result occurs if one – and only one – of the gate’s inputs is true. If both inputs are false (i.e. LOW or 0) or both inputs are true, the output is false.

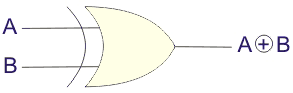
 

**Simplified expression**



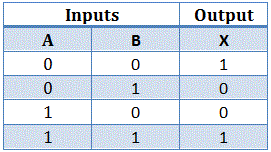
From this Boolean expression, one can easily realize the logical circuit of an XOR gate, and this will be as shown,  


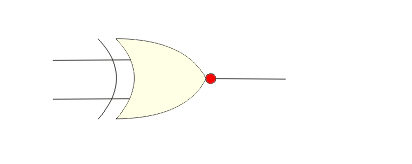
## **Logical Symbol of XOR Gate**

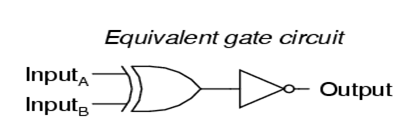
An XOR gate is logically represented as,  


## **XNOR Gate Truth Table**

The [truth table](https://www.electrical4u.com/truth-table/) of the **XNOR gate** is shown below:



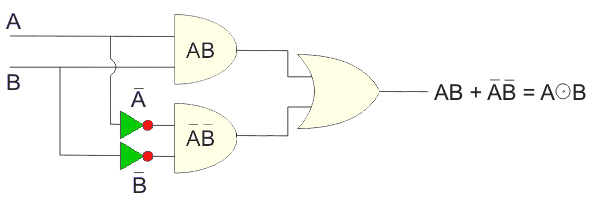
The symbol of the XNOR gate:  


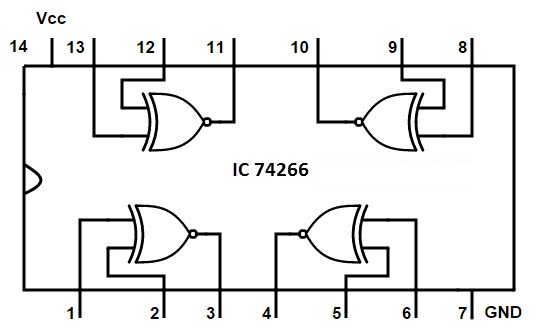


**Expression**

A ⊙ B = AB + ĀB ̅.

## **XNOR Gate Circuit Diagram**

The expression of XNOR operation can be realized by using two [NOT gates](https://www.electrical4u.com/not-gate/), two [AND gates](https://www.electrical4u.com/logical-and-gate/), and one [OR gate](https://www.electrical4u.com/logical-or-gate/) as followers,  




**Lab Task:**

**Task 1:**

**Design 3 input xor and xnor gate and write its truth table and draw the circuit diagram on the software.**

#### **Lab Task#2:**

Implement the following logic circuit on logic trainer, and write Boolean Expression

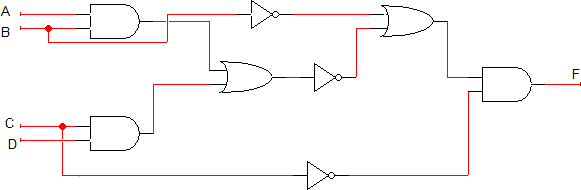


Figure 9: Combinational Circuit

X = (((A.B) + (C.D))’+ B’). C’

**Lab Task#3**

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 Write the Boolean expression for each of the logic circuits in Figure 2.2. Also implement the given circuits on breadboard and draw Truth tables:

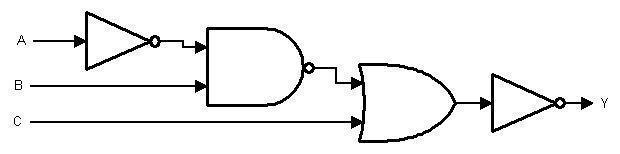


Figure 10: Combinational Circuit

X = ((A’.B)’ +C )’

**Lab Task#4**

Draw a circuit diagram corresponding to the following Boolean expression and implement it on breadboard:

1. (A + B)(B + C)
2. (AB + C)D
3. ((A + B’C)(A + BC))’
4. A’BC + AB’C + ABC’ + (ABC)’
5. (A’ + BC)’

#### **Lab Task#5**

Transform the given diagram figure 9 of logic circuit to new logic diagram using NAND /NOR gates only, in the space given below. Show complete working. Implement the transformed logic circuit on logic trainer.

QUOTE OF THE WEEK:

There are no shortcuts to any place worth going